CLAIMS

[Claim 1] An MIS-type field-effect transistor characterized in comprising:

a base layer;

a strained active semiconductor layer formed on said base layer;

a gate insulating film formed on said active semiconductor layer;

a gate electrode formed on said gate insulating film; and

a source/drain region formed in portions on both sides of said gate electrode inside said active semiconductor layer;

wherein

an interface between said base layer and said active semiconductor layer is at a depth of $2T_p$ or less from the surface, where T_p is the depth of maximum concentration of an impurity introduced for forming said source/drain region.

[Claim 2] An MIS-type field-effect transistor characterized in comprising:

a base layer;

a strained active semiconductor layer formed on said base layer;

a gate insulating film formed on said active semiconductor layer;

a gate electrode formed on said gate insulating film;

a source/drain region formed in portions on both sides of said gate electrode inside said active semiconductor layer; and

a gate side wall formed on the lateral face of said gate

electrode; wherein

a portion under said gate side wall and said gate electrode of said active semiconductor layer has a greater film thickness than any other portion; and

an interface between said base layer and said active semiconductor layer is at a depth of $2T_p$ or less from the surface of a region disposed other than under said gate side wall and said gate electrode of said active semiconductor layer, where T_p is the depth of maximum concentration of an impurity introduced for forming said source/drain region.

[Claim 3] An MIS-type field-effect transistor characterized in comprising:

a base layer;

a strained active semiconductor layer formed on said base layer;

a gate insulating film formed on said active semiconductor layer;

a gate electrode formed on said gate insulating layer; and

a built-up layer provided with a source/drain region and formed on said active semiconductor layer on both sides of said gate electrode; wherein

said built-up layer has a film thickness of $3T_p$ or greater, where T_p is the depth of maximum concentration of an impurity introduced for forming said source/drain region.

[Claim 4] The MIS-type field-effect transistor according to claim 3, characterized in that the film thickness of said built-up layer is $5T_p$.

[Claim 5] The MIS-type field-effect transistor according to any of claims 1 through 4, characterized in that said base layer is a semiconductor layer having the composition $Si_{1-x-y}Ge_xC_y$ (wherein $0 \leq x \leq 1$, $0 \leq y \leq 1$, and $0 < x + y \leq 1$).

[Claim 6] The MIS-type field-effect transistor according to any of claims 1 through 4, characterized in that said base layer is an Si layer.

[Claim 7] The MIS-type field-effect transistor according to any of claims 1 through 6, characterized in that said base layer is a semiconductor layer, and an insulator layer is formed underneath said base layer.

[Claim 8] The MIS-type field-effect transistor according to any of claims 1 through 4, characterized in that said base layer is an insulator layer.

[Claim 9] The MIS-type field-effect transistor according to any of claims 1 through 8, characterized in that said active semiconductor layer is a group IV semiconductor layer.

[Claim 10] The MIS-type field-effect transistor according to any of claims 1 through 5, 7, and 8, characterized in that said active semiconductor layer is an Si layer.

[Claim 11] The MIS-type field-effect transistor according to any of claims 1 through 8, characterized in that said active semiconductor layer is a semiconductor layer having the composition $Si_{1-x-y}Ge_xC_y$ (wherein $0 \leq x \leq 1$, $0 \leq y \leq 1$, and $0 < x + y \leq 1$).

[Claim 12] The MIS-type field-effect transistor according to claim 11, characterized in comprising an Si layer with a film thickness of 10 nm or less between said active semiconductor

layer and said gate insulating film.

[Claim 13] The MIS-type field-effect transistor according to any of claims 1 through 12, characterized having a gate length of 0.4 μm or less.

[Claim 14] The MIS-type field-effect transistor according to any of claims 1 through 13, characterized in that said source/drain region is formed by an ion implantation method.

[Claim 15] The MIS-type field-effect transistor according to any of claims 1 through 13, characterized in that said source/drain region is formed by a plasma doping method.

[Claim 16] The MIS-type field-effect transistor according to any of claims 1 through 13, characterized in that said source/drain region is formed by a gas-phase doping method.

[Claim 17] The MIS-type field-effect transistor according to any of claims 1 through 16, characterized in that a portion of said source/drain region near the gate electrode is a region of low impurity concentration.